

A/D Converters cont.

Errors in A/D Converters

Errors that may occur in A/D converters are defined and measured in terms of the location of the actual transition points in relation to their locations in the ideal transfer characteristic. These are discussed below.

Quantization Uncertainty

Unlike a D/A converter, where there exists a unique analog value for each digital code, each digital output code is valid over a range of analog input values. Analog inputs within a given discrete range are represented by the same digital output code, usually assigned to the nominal mid-range analog value. There is, therefore, an inherent quantization uncertainty of $\pm 1/2$ LSB (least-significant bit), in addition to any other actual conversion errors. This is shown in Figure 6b.

Unipolar Offset

Note that in the ideal transfer function, the first transition should ideally occur $1/2$ LSB above analog common. The unipolar offset is the deviation of the actual transition point from the ideal first transition point. This is shown in Figure 7a.

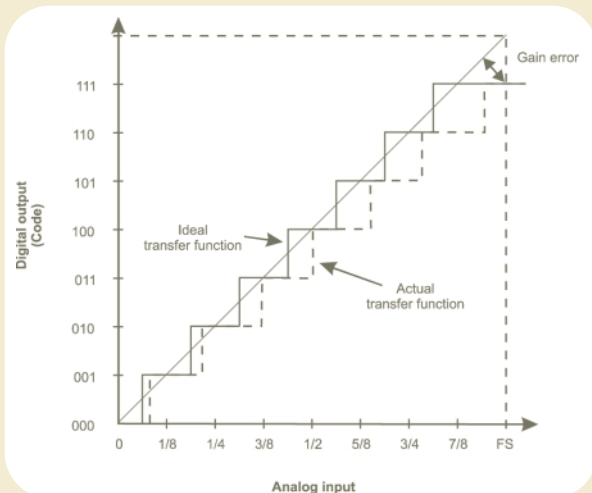


Figure 8a - Unipolar Gain Error

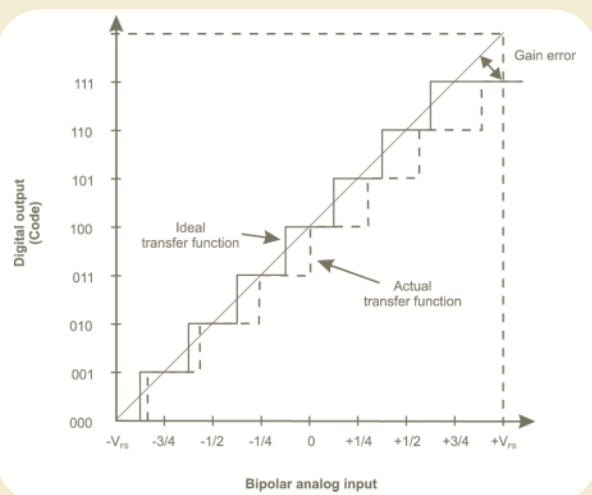


Figure 8b - Bipolar Gain Error

Figure 8 - 3-bit A/D Converter Transfer Functions with Gain Errors

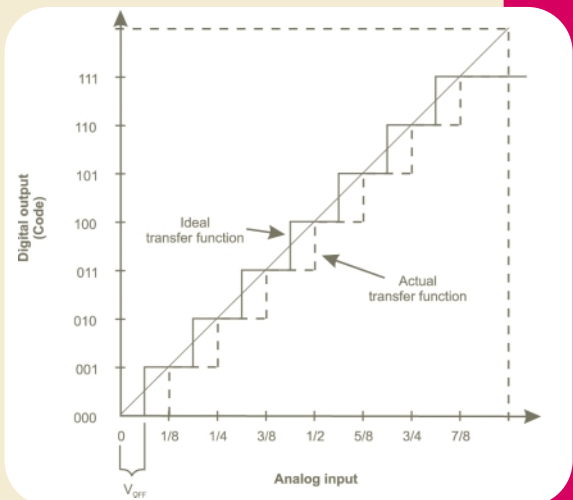


Figure 7a - Unipolar Offset Error

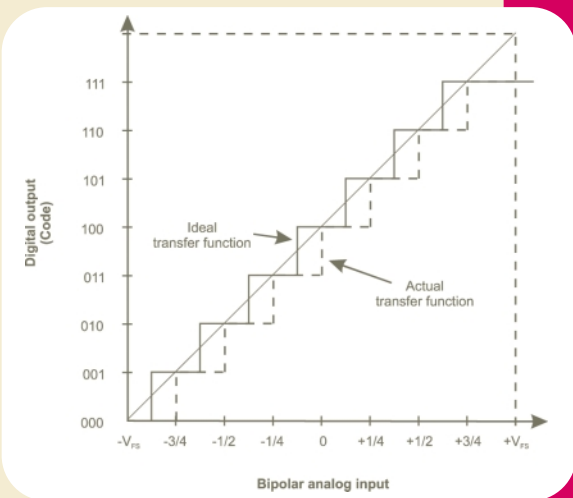


Figure 7b - Bipolar Offset Error

Figure 7 - 3-bit A/D Converter Transfer Functions with Offset Errors

Bipolar Offset

As seen in Figure 7b the transfer function for an ideal bipolar ADC resembles the unipolar transfer function, except that it is offset by the negative full-scale voltage (-FSV). Offset adjustment of a bipolar A/D converter is set so that the first transition occurs at $1/2$ LSB above -FSV, while the last transition occurs at $-3/2$ LSB below +FSV. Because of non-linearity, a device with perfectly calibrated end points may have an offset error at analog common. This is known as the bipolar offset error and is shown in Figure 7b.

Unipolar and Bipolar Gain Errors

The gain, or scale, factor is the number which establishes the basic conversion relationship between the analog input values and the digital output codes, e.g. 10 V full-scale. It represents the straight-line slope of the ideal transfer characteristic.

The gain error is defined as the difference in full scale values between the ideal and the actual transfer function when any offset errors are adjusted to zero. It is expressed as a percentage of the nominal full scale value or in LSBs.

Gain error affects each code in an equal ratio. Unipolar and bipolar gain errors are shown in Figure 8.

Offset and Gain Drift

Offset and gain errors are usually adjustable to zero with calibration, however this calibration is only valid at the temperature at which it was made.

Changes in temperature result in a non-zero offset and gain error, known as offset drift and gain drift. These values, specified in ppm / deg C, represent the ADC's sensitivity to temperature changes.

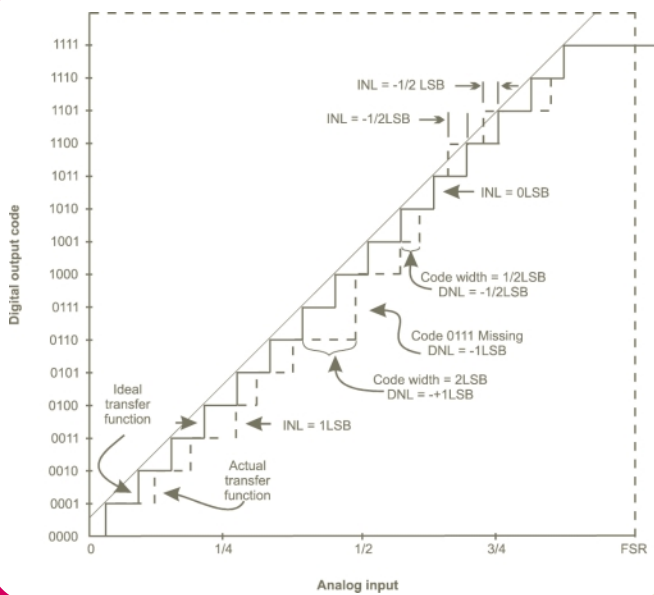


Figure 9a - Integral Non-linearity Errors Specified as Low-Side Transition

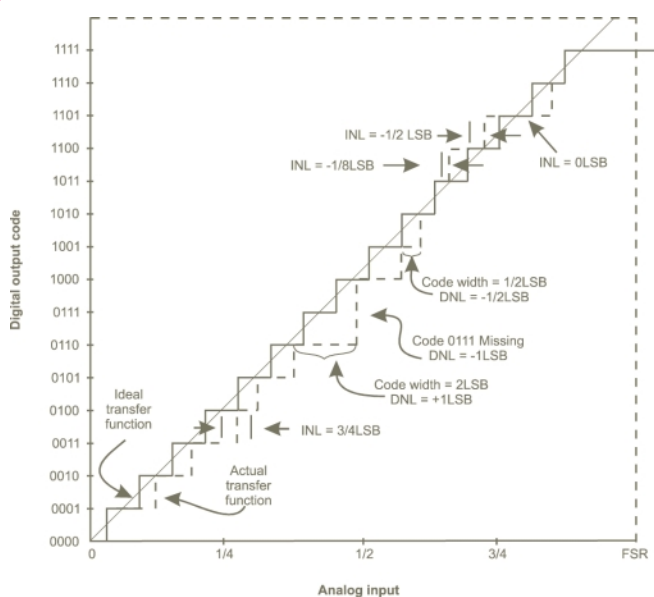


Figure 9b - Integral Non-linearity Errors Specified as Center-of-Code Transition

Figure 9 - Transfer Function of a 4-bit A/D Converter with Integral Non-Linearity and Differential Non-Linearity Errors

than -1 LSB. In the worst case, where the code width is equal to or very near zero, then a missing code may result. This means that there is no voltage in the entire full-scale voltage range that can cause the code to appear.

In Figures 9a and 9b, the code-width of code 0110 is 2 LSBs, resulting in a differential non-linearity of +1 LSB. As the code-width of the code 1001 is 1/2 LSB, this code has a DNL of -1/2 LSB. Also the code 0111 does not exist for any input voltage. This means that code 0111 has -1 DNL and the A/D converter has at least one missing code.

Often, instead of a maximum DNL specification, there will be a simple specification of monotonicity or no missing codes. For a device to be monodic, the output must either increase or remain constant as the analog input increases. Monodic behavior requires that the differential non-linearity be more positive than -1 LSB. However, the differential non-linearity error may still be more positive than +1 LSB. Where this is the case the resolution for that particular code is reduced.

Integrating A/D Converters

Linearity Errors

With most ADCs the gain and offset specifications are not the most critical parameters that determine an A/D converter's usefulness for a particular application, since in most cases they can be calibrated out in software and/or hardware. The most important error specifications are those which are inherent in the device and cannot be eliminated.

Ideally, as the analog input voltage of an A/D converter is increased, the digital codes at the output should also increase linearly. The ideal transfer function of the analog input voltage verses the digital output code would show a straight line.

Deviations from the straight line are specified as non-linearities. The most important of these, (because they are errors which cannot be removed), are integral non-linearity and differential non-linearity errors. The transfer characteristics of a 4-bit A/D converter showing differential and integral linearity errors are shown in Figure 9a and Figure 9b.

Integral Non-Linearity (INL)

This is the deviation of the actual transfer function from the ideal straight line. This ideal line may be drawn through the points where the codes begin to change (low-side transition or LST), as shown in Figure 9a, or through the center of the ideal code widths (center-of-code or CC), as shown in Figure 9b.

Most A/D converters are specified by low-side-transition INL. Thus the line is drawn from the point 1/2 LSB on the vertical axis at zero input to the point 3/2 LSB beyond the last transition at full-scale input. The deviation of any transition from its corresponding point on that straight line is the INL of the transition.

In Figure 9a the transition to code 0100 is shifted to the right by 1 LSB, meaning that the LST of code 0100 has an INL of +1 LSB. In the same figure the transition to code 1101 is shifted left by 1/2 LSB, meaning that the LST of code 1101 has an INL of -1/2 LSB.

When the ideal transfer function is drawn for center-of-code (CC) integral non-linearity specification, as shown in Figure 5.9(b), the INL of each transition may be different. Where the digital code 1101 previously had -1/2 LSB of LST INL, it now has 0 LSB of CC INL. Similarly the code 1011 has -1/8 LSB of CC INL where it previously had 0 LSB of LST INL.

The INL is an important figure because the accurate translation from the binary code to its equivalent voltage is then only a matter of scaling.

Differential Non Linearity (DNL)

In an ideal A/D converter the midpoints between code transitions should be 1 LSB apart. Differential non-linearity is defined as the deviation in code width from the ideal value of 1 LSB. Therefore, an ideal A/D converter has a DNL of 0 LSB, while practically this would be $\pm 1/2$ LSB.

If DNL errors are large, the output code widths may represent excessively large or small ranges of input voltages. Since codes do not have a code width less than 0 LSB, the DNL can never be less

Memory (FIFO) Buffer

A characteristic of high speed A/D boards is the inclusion of on-board memory or I/O in the form of a FIFO (First In First Out) buffer or a pair of buffers. These range in size from 16 bytes to 64 Kbytes.

The FIFO buffer(s) form a fast temporary memory area. For small FIFOs, the buffer is addressed as I/O. Larger FIFOs are actually mapped into the memory address space of the host PC. Samples can therefore be collected up to the maximum size of the buffer without actually having to perform any data transfers. Where more samples are required, existing data in the buffer must be transferred to other parts of the main memory, or written to hard disk, before it gets overwritten.

FIFO buffering is particularly useful in situations where the host computer is using polled I/O or interrupts to transfer data, and might not be able to respond quickly enough to transfer the current sample, before it is overwritten by a subsequent sample. This would typically occur when the host computer is running a multi-tasking operating system such as Windows or OS/2, where there are inherent interrupt latencies or a large number of tasks being performed.

The FIFO buffer also has the effect of evening-out variations in DMA response times, helping to guarantee full-speed operations even with substandard PC/AT clones.

On-board FIFOs, when used in conjunction with specific data techniques such as polled I/O, interrupts, DMA or repeat string instructions, can greatly improve the throughput of A/D boards.

Timing Circuitry

To perform multiple analog-to-digital conversions automatically, at precisely-defined time intervals, A/D boards are equipped with timing circuitry whose principal responsibility is to generate the strobe signals which allow the components of the analog input circuitry to perform their respective functions efficiently and correctly.

Clocking circuits are made up of a frequency source, which is either an on-board oscillator between 400 kHz and 10 MHz or an external user-supplied signal, and a pre-scaler/divider network, typically a counter/timer chip, that slows the clock signal down to more usable values. The clock frequency can be as low as 1 Hz or up to the maximum throughput of the board.

A/D conversions are started by triggers, either by a software trigger (writing to an on-board register), or an external hardware trigger. Data conversions can be synchronized with external events with the use of external clock frequency sources and external triggers. The external trigger event is usually in the form of a digital or analog signal and will begin the acquisition depending on the active edge, if the trigger is a digital signal, or the level and slope if the trigger is an analog signal.

In performing an analog-to-digital conversion cycle on a single input channel, the timing circuitry must ensure the following steps are performed:

- Once the channel/gain array has been initialized, the timing circuitry increments to the next channel/gain pair. The next channel to be sampled is output to the address lines of the input multiplexer and the required gain setting is output to the programmable gain amplifier (PGA). The sample-and-hold (S/H) is put into sample mode.
- The timing circuitry must wait for the input multiplexer to settle, then for the PGA output delay time and lastly for any S/A delay.
- The S/H is put into hold mode. The timing circuitry must wait for the duration of the aperture time of the S/H for the signal to become stable at the output of the S/H.
- A start conversion trigger is issued to the A/D converter.
- The timing circuitry waits for the end of conversion signal from the A/D converter to become active.
- The available data is then strobed from the A/D converter into a data buffer or a FIFO, from where it is usually accessible by the host computer.
- If simultaneous sampling is available on the A/D board, the timing circuitry generates the necessary sequence of strobes to the input S/H devices, so that all channels are sampled at the beginning of the sampling cycle, before the data is passed to the rest of the analog input circuitry.

Total throughput, for multiple conversions on different channels, is often increased by overlapping parts of this cycle. For example, while the A/D converter is busy converting the S/H output, the next channel/gain pair can be output to the multiplexer and PGA, so that their settling and delay times are overlapped with the A/D conversion time.

The timing circuitry may also include a block sampling mode which allows blocks of samples to be collected at regular intervals at the A/D board's maximum sampling rate.

Expansion Bus Interface

The bus interface provides the control circuitry and signals used to transfer data from the board to the PC's memory or for sending configuration information (e.g. channel/gain pairs) or other commands (e.g. software triggers) to the board.

It includes:

- The plug-in connector which provides the hardware interface for connecting all control and data signals to the expansion bus (e.g. ISA, EISA etc) of the host computer.
- The circuitry which determines the base address of the board. This is usually a selectable DIP switch and defines the addresses of each memory and I/O location on the A/D board.
- The source and level of interrupt signals generated. Interrupt signals can be programmed to occur at the end of a single conversion or a DMA block. The configuration of the interrupt levels used is commonly selected by on-board links.
- DMA control signals and the configuration of the DMA level(s) used. The configuration of the DMA levels used is typically selected by on-board links.
- Normal I/O to and from I/O address locations on the board.
- Wait state configuration for use in machines with high bus speeds or with non-standard timing. The number of wait states is usually configurable by on-board links.